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- 1 Handling irreducible loops: optimized node splitting versus DJ-graph**  
 Sebastian Unger, Frank Mueller  
 July 2002 **Transactions on Programming Languages and Systems (1)**  
**Publisher:** ACM  
 Full text available: Pdf (386.11 KB) [Additional Information: full citation, abstract, ref.](#)  
**Bibliometrics:** Downloads (6 Weeks): 7, Downloads (12 Months): 52, Citation (

This paper addresses the question of how to handle irreducible regions which has become even more relevant for contemporary processors since recent processors highly rely on instruction scheduling. The contributions ...

**Keywords:** Code optimization, compilation, control flow graphs, instruction scheduling, irreducible flowgraphs, loops, node splitting, reducible flowgraphs

- 2 Inter-cluster communication in VLIW architectures**  
 A. S. Terschko, H. Corporaal  
 June 2007 **Transactions on Architecture and Code Optimization (TACO)**  
**Publisher:** ACM  
 Full text available: Pdf (996.47 KB) [Additional Information: full citation, abstract, ref.](#)  
**Bibliometrics:** Downloads (6 Weeks): 24, Downloads (12 Months): 162, Citation (

The traditional VLIW (very long instruction word) architecture with a single cluster can scale up well to address growing performance demands on embedded processors by splitting a VLIW processor in smaller clusters, which are ...

**Keywords:** Instruction-level parallelism, VLIW, clock frequency, cluster architecture, scheduler, intercluster communication, optimizing compiler, pipelining, parallel processing

- 3 Symbolic transfer function-based approaches to certified compilation**  
 Xavier Rival  
 January 2004 **POPL '04: Proceedings of the 31st ACM SIGPLAN-SIGACT symposium on Programming Languages**  
**Publisher:** ACM  
 Full text available: Pdf (212.73 KB) [Additional Information: full citation, abstract, ref.](#)  
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We present a framework for the certification of compilation and of compiler approach uses a symbolic transfer functions-based representation of programs that source and compiled programs present similar behaviors. This checker

**Keywords:** abstract interpretation, certification, compilation, static analysis

Also published in:

January 2004 **SIGPLAN Notices** Volume 39 Issue 1


- 4 [Synthesis of Heterogeneous Distributed Architectures for Memory-In](#)  
Chao Huang, Sriyaths Ravi, Anand Raghunathan, Niraj K. Jha  
November 2003 **ICCAD '03: Proceedings of the 2003 IEEE/ACM International Conference on Computer-aided design**

**Publisher:** IEEE Computer Society


Full text available:  Pdf (756.95 KB) Additional Information: [full citation](#), [abstract](#), [ref: full text](#)

**Bibliometrics:** Downloads (6 Weeks): 5, Downloads (12 Months): 26, Citation (

Memory-intensive applications present unique challenges to an ASIC designer's choice of memory organization, memory size requirements, bandwidth and area. The high potential of single-chip distributed logic-memory architectures

- 5 [Reducing the cost of conditional transfers of control by using compar](#)  
 William Krehling, Stephen Hines, David Whalley, Gary Tyson  
July 2006 **LCTES '06: Proceedings of the 2006 ACM SIGPLAN/SIGBED conference on compilers, and tool support for embedded systems**

**Publisher:** ACM

Full text available:  Pdf (124.43 KB) Additional Information: [full citation](#), [abstract](#), [ref: full text](#)

**Bibliometrics:** Downloads (6 Weeks): 3, Downloads (12 Months): 21, Citation (

A significant portion of a program's execution cycles are typically dedicated to conditional transfers of control. Much of the research on reducing the cost of such has focused on the branch, while the comparison has been largely ...



**Keywords:** branch, comparison, compiler, optimization

Also published in:

July 2006 **SIGPLAN Notices** Volume 41 Issue 7

- 6 [Hardware/Software Design Space Exploration for a Reconfigurable F](#)  
Alberto La Rosa, Luciano Lavagno, Claudio Passerone  
March 2003 **DATE '03: Proceedings of the conference on Design, Automation and Test in Europe - Volume 1** . Volume 1

**Publisher:** IEEE Computer Society



Full text available:  Publisher Site ,  Pdf (103.11 KB) Additional Information: [full citation](#), [abstract](#), [ref: full text](#), [index text](#)

**Bibliometrics:** Downloads (6 Weeks): 0, Downloads (12 Months): 25, Citation (

This paper describes an approach to hardware/software design space exploration for reconfigurable processors. The existing compiler tool-chain, because of its reliance on instructions, needs to be extended in order to offer developers an easy



- 7 [Proceedings of the 2009 Conference on Asia and South Pacific Design Automation](#)  
 Kazutoshi Wakabayashi  
 January 2009 **ASP-DAC '09: Proceedings of the 2009 Conference on Asia and South Pacific Design Automation**  
**Publisher:** IEEE Press  
**Additional Information:** [full citation](#), [abstract](#)  
**Bibliometrics:** Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Citation

On behalf of the Organizing Committee, I would like to invite you to attend the Asia and South Pacific Design Automation Conference 2009 (ASP-DAC 2009), being held in Yokohama, Japan, from January 19 through 22, 2009, jointly with the E

- 8 [Design and Implementation of the AEGIS Single-Chip Secure Processor](#)  
 Random Functions  
 G. Edward Suh, Charles W. O'Donnell, Ishan Sachdev, Srinivas Devadas  
 June 2005 **ISCA '05: Proceedings of the 32nd annual international symposium on Computer Architecture**  
**Publisher:** ACM  
 Full text available:  Pdf (288.96 KB) **Additional Information:** [full citation](#), [abstract](#), [ref](#)  
**Bibliometrics:** Downloads (6 Weeks): 29, Downloads (12 Months): 135, Citation

Secure processors enable new applications by ensuring private and authentic data even in the face of physical attack. In this paper we present the AEGIS architecture, and evaluate its RTL implementation on FPGAs. By using ...

Also published in:  
 May 2005 **SIGARCH Computer Architecture News** Volume 33 Issue 2

- 9 [Improving Program Efficiency by Packing Instructions into Registers](#)  
 Stephen Hines, Joshua Green, Gary Tyson, David Whalley  
 June 2005 **ISCA '05: Proceedings of the 32nd annual international symposium on Computer Architecture**  
**Publisher:** ACM  
 Full text available:  Pdf (316.46 KB) **Additional Information:** [full citation](#), [abstract](#), [ref](#)  
**Bibliometrics:** Downloads (6 Weeks): 4, Downloads (12 Months): 54, Citation

New processors, both embedded and general purpose, often have conflicts involving space, power, and performance. Architectural features and compilers target one or more design goals at the expense of the others. ...

Also published in:  
 May 2005 **SIGARCH Computer Architecture News** Volume 33 Issue 2

- 10 [Behavioral synthesis techniques for intellectual property protection](#)  
 Farinaz Koushanfar, Inki Hong, Miodrag Potkonjak  
 July 2005 **Transactions on Design Automation of Electronic Systems** Issue 3  
**Publisher:** ACM  
 Full text available:  Pdf (439.81 KB) **Additional Information:** [full citation](#), [abstract](#), [ref](#)  
**Bibliometrics:** Downloads (6 Weeks): 40, Downloads (12 Months): 276, Citation

We introduce dynamic watermarking techniques for protecting the value CAD and compilation tools and reusable design components. The essence the addition of a set of design and timing constraints which ...


**Keywords:** Intellectual property protection, behavioral synthesis, water

# 11 [A Compiler Scheme for Reusing Intermediate Computation Results](#)

Yonghua Ding, Zhiyuan Li

March 2004 **CGO '04**: Proceedings of the international symposium on Code optimization: feedback-directed and runtime optimization


**Publisher:** IEEE Computer Society

Full text available:  Pdf (178.85 KB) Additional Information: [full citation](#), [abstract](#), [ref](#)

**Bibliometrics:** Downloads (6 Weeks): 1, Downloads (12 Months): 20, Citation (

Recent research has shown that programs often exhibit value locality. So code segment, although executed repeatedly in the program, takes only values as input and, naturally, generates a small number of ...

# 12 [Application specific compiler/architecture codesign: a case study](#)

 Oliver Wahlen, Timan Glöckler, Achim Nohl, Andreas Hoffmann, Rainer Lauß  
July 2002 **LCTES/ SCOPES '02**: Proceedings of the joint conference on La

tools for embedded systems: software and compilers for embed

**Publisher:** ACM

Full text available:  Pdf (290.01 KB) Additional Information: [full citation](#), [abstract](#), [ref](#)

**Bibliometrics:** Downloads (6 Weeks): 6, Downloads (12 Months): 48, Citation (


This paper proposes an architecture exploration methodology for applic set processors (ASIPs) including a C compiler and a VHDL model in the given application the target architecture is an instance of ...

**Keywords:** ASIP, architecture exploration, retargetable compiler


Also published in:

July 2002 **SIGPLAN Notices** Volume 37 Issue 7

# 13 [LIBRA—a library-independent framework for post-layout performanc](#)

 Bic Chung-Yang Huang, Yucheng Wang, Kwang-Ting Chen

April 1998 **ISPD '98**: Proceedings of the 1998 international symposium on  
**Publisher:** ACM

Full text available:  Pdf (906.11 KB) Additional Information: [full citation](#), [abstract](#), [ref](#)


**Bibliometrics:** Downloads (6 Weeks): 0, Downloads (12 Months): 13, Citation (

In this paper we present a post-layout timing optimization framework w independent such that it can take the logic-optimized Verilog file as its i prototype interface which can communicate with any vendor's ...

# 14 [Coordinated transformations for high-level synthesis of high perform](#)



 blocks

Sumit Gupta, Nick Savaiu, Nikil Dutt, Rajesh Gupta, Alex Nicolau, Timothy Shai Botem

June 2002 **DAC '02**: Proceedings of the 39th conference on Design autom:  
**Publisher:** ACM  
 Full text available:  Pdf (144.01 KB) **Additional Information:** full citation, abstract, ref:  
**Bibliometrics:** Downloads (6 Weeks): 0, Downloads (12 Months): 11, Citation (



High performance microprocessor designs are partially characterized by consisting of a large number of operations that are packed into very few cycle) with little or no resource constraints but tight bounds on the ...

**Keywords:** high-level synthesis, microprocessor design



15 Combined instruction and loop parallelism in array synthesis for FPG  
 Steven Derrien, Sanjay Rajopadhye, Susmita Sur Kolay  
 September 2001 **ISSS '01**: Proceedings of the 14th international symposium  
**Publisher:** ACM  
 Full text available:  Pdf (188.22 KB) **Additional Information:** full citation, abstract, ref:  
**Bibliometrics:** Downloads (6 Weeks): 3, Downloads (12 Months): 6, Citation C

Compiling perfect, uniform dependence loops to fpga based co-process processor pe arrays where a pe executes one instance of the loop body develop a transformation framework in which the derived ...

**Keywords:** instruction level parallelism, programmable logic, regular p

16 Recursive circuit clustering for minimum delay and area  
 Mehrdad Eslami Dehkordi, Stephen D. Brown  
 February 2003 **FPGA '03**: Proceedings of the 2003 ACM/ SIGDA eleventh int  
 Field programmable gate arrays  
**Publisher:** ACM  
 Full text available:  Pdf (187.05 KB) **Additional Information:** full citation, abstract  
**Bibliometrics:** Downloads (6 Weeks): 1, Downloads (12 Months): 9, Citation C

We present an effective recursive algorithm for circuit clustering for del which is applicable to FPGAs. At the highest level of clustering, the circ modified single-level clustering algorithm. A cluster ...

17 A scalable wide-issue clustered VLIW with a reconfigurable intercon  
 Osvaldo Colavin, Davide Fizzo  
 October 2003 **CASES '03**: Proceedings of the 2003 international conference  
 architecture and synthesis for embedded systems  
**Publisher:** ACM  
 Full text available:  Pdf (365.26 KB) **Additional Information:** full citation, abstract, ref:  
**Bibliometrics:** Downloads (6 Weeks): 2, Downloads (12 Months): 30, Citation (

Clustered VLIW architectures have been widely adopted in modern emb applications for their ability to exploit high degrees of ILP with reasonab and silicon costs. Studies have however shown limited performance ...

**Keywords:** IDCT, clustered VLIW, modulo scheduling, reconfigurable c

### 18 A Scalable Application-Specific Processor Synthesis Methodology

Fe: Sun, Srivaths Ravi, Anand Raghunathan, Niraj K. Jha

November 2003 **ICCAD '03: Proceedings of the 2003 IEEE/ACM international Computer-aided design**

**Publisher:** IEEE Computer Society

Full text available:  Pdf (472.11 KB) Additional Information: full citation, abstract, ref

**Bibliometrics:** Downloads (6 Weeks): 4, Downloads (12 Months): 31, Citation (


Custom processors based on application-specific or domain-specific instruction set architectures are often used to implement critical architectural blocks in custom chips. While several advances have been made in custom processor ...

### 19 Selective code transformation for dual instruction set processors

Sheayun Lee, Jaemin Lee, Chang Yun Park, Sang Lyul Min

May 2007 **Transactions on Embedded Computing Systems (TECS)**, 1

**Publisher:** ACM

Full text available:  Pdf (342.64 KB) Additional Information: full citation, abstract, ref

**Bibliometrics:** Downloads (6 Weeks): 11, Downloads (12 Months): 85, Citation

Embedded systems are often constrained in terms of both code size and of a limited amount of available memory and real-time nature of application processor, which supports a reduced instruction set (RISC) ...

**Keywords:** Dual instruction set processors, mixed-width instruction set architecture

### 20 Proceedings of the 2005 conference on Asia South Pacific design automation

Ting-Ao Tang

January 2005 **ASP-DAC '05: Proceedings of the 2005 conference on Asia South Pacific design automation**

**Publisher:** ACM

Additional Information: full citation, abstract

**Bibliometrics:** Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Citation

It's a great pleasure for me on behalf of the Organizing Committee to welcome you to the Asia and South Pacific Design Automation Conference (ASP-DAC 2005) in the city of DAC, DATE, and ICCAD. ASP-DAC 2005 will be held in Hotel ...

Result

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